Nyquist-criterion based design of a CT $\Sigma\Delta$-ADC with a reduced number of comparators

Jeroen De Maeyer, Pieter Rombouts and Ludo Weyten

This document is an author's draft version submitted for publication to INTEGRATION-THE VLSI JOURNAL.
The actual version was published as:
J. De Maeyer, P. Rombouts and L. Weyten, "Nyquist-criterion based design of a CT Sigma Delta-ADC with a reduced number of comparators," INTEGRATION, the VLSI journal, vol. 42, No. 1, pp. 61-67, Jan. 2009

Nyquist-criterion based design of a CT $\Sigma\Delta$-ADC with a reduced number of comparators

Jeroen De Maeyer, Pieter Rombouts and Ludo Weyten

Electronics and Information Systems Lab., Ghent University,
St.-Pietersnieuwstraat 41, 9000 Gent, Belgium

Abstract

In this paper we present a prototype continuous time $\Sigma\Delta$-modulator in a 0.35 μm technology. The circuit has a 6-bit internal quantizer. Through the combination of a modified architecture and comparator interpolation this high quantizer resolution is achieved with only 15 comparators. However, it turns out that this approach imposes a severe speed constraint on the analog adder circuit.

The modulator consists of a 3rd order loop and special care was taken in the design of the loop filter. The presented design has two particular features. First an explicit and controlled delay of 0.25 times the sampling period is introduced in the loop. Second, the Nyquist stability criterion and the vector gain margin are adopted to design a robustly stable modulator loop filter. This way our modulator does not require any tuning or trimming of the filter coefficients. Measurement results show a Peak SNR of 82 dB and a dynamic range of 85 dB for a bandwidth of 1.5 MHz.

Key words: analog-to-digital conversion, Continuous time Sigma Delta modulation

1 Introduction

Sigma Delta modulation A/D converters are proven building blocks and are frequently used in radio receiver systems. However, for portable applications the power consumption is under constant pressure. In this aspect continuous time sigma delta modulators are considered superior over their discrete time counterparts [1, 2]. Moreover these circuits incorporate an inherent anti-aliasing filter, further simplifying the overall receiver architecture [1–4]. Unfortunately these circuits are sensitive to clock jitter [5–7]. One possible way to improve this, is to use a modified pulse shape for the feedback DAC. This way, the Switched-capacitor (SCR) [4, 8, 9] and the sinusoidal [10] feedback pulse

have been presented. However, the SCR-pulse increases the slew-rate requirements on the analog parts and the sinusoidal pulse is difficult to implement. Another approach, which is followed in this work, would be to use a standard non-return-to-zero feedback pulse and to decrease the quantization step (Δ) of the internal quantizer, since the jitter error is proportional to Δ [11–14]. However, in prior designs the resolution of the internal quantizer in a continuous time $\Sigma\Delta$-modulator was limited to 4 or 5 bit, e.g. [12]. In this paper the design of a modulator with an equivalent quantizer resolution of 6-bit is investigated. In a straightforward architecture, such a high quantizer resolution would be difficult to achieve, because it would require 63 comparators. Thus the chip area and the capacitive loading on the preceding circuit blocks would become unacceptable. However, by the combination of a modified architecture [14, 15] and comparator interpolation the total number of comparators is reduced to 15.

An additional problem due to the high-quantizer resolution is the need for a dynamic element matching technique to linearize the feedback DAC. Because of this, a significant delay in the feedback path of the loop is inevitable. It is well known that this delay increases the order of the modulator and may cause stability problems [12, 13, 16, 17]. In [12, 13, 17] this problem is tackled by adding an extra direct path between the output of the modulator and the input of the quantizer. However, in our case of a 6-bit quantizer this approach would require an additional 6-bit DAC, which makes this option less interesting. Moreover such a structure requires matching of the sampling period and the integrator time constants of the loop filter. Therefore this extra DAC was avoided. Instead, we used an explicit synchronisation in the feedback path to set the loop delay to a known and controlled value. In the design of the loop filter this loop delay is taken into account. In our design this loop filter is of third-order. The modulator loop filter coefficients are then determined through the Nyquist-criterion approach described in [18]. This way a modulator which is robustly stable against most nonidealities is achieved. Unlike most prior multi-bit designs [11–13] this is achieved without tuning or trimming circuitry.

The rest of the paper is structured as follows. In section 2 the architecture for reducing the number of comparators [14] is reviewed. Section 3 is dedicated to the Nyquist criterion design strategy. Next, in section 4 the circuit level design is addressed. Finally, before drawing the conclusions, measurement and evaluation results are discussed in section 5.

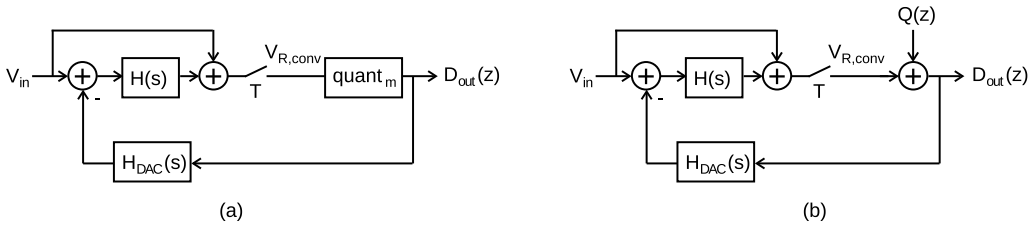

Figure 1. (a) Typical continuous time ΣΔ-modulator architecture and (b) its linearized model.

2 Architecture

Figure 1 shows a typical diagram of a conventional continuous time ΣΔ-modulator [1, 13], with its linearized model where the quantiser is replaced by an additive quantization noise signal Q. Such a modulator consists of a closed loop with a loop-filter and a quantiser. There is also a feedforward branch directly connecting the modulator-input signal V_{in} to the input of the quantiser. This improves the distortion of the overall modulator [19] by reducing the voltage swing at the internal nodes. However, the anti-aliasing filtering properties are deteriorated by this feedforward branch [3]. In the presented circuit anti-aliasing was not considered of primary importance and therefore this feedforward branch is included, but it is not essential for any of the techniques presented in this work and may be removed, if anti-aliasing filtering is an important issue.

In such a circuit the signal at the input of the internal quantizer ($V_{R,conv}$) is given by:

$$V_{R,conv}(z) = [STF(s)V_{in}(s)]^* + NTF(z)Q(z) \tag{1}$$

Here, NTF denotes the noise transfer function while STF stands for the signal transfer function as defined in [3]. Concentrating on this first term, the input signal $V_{in}(s)$ is propagated through the STF after which it is sampled. This sampling operation is indicated in short by the *-operator [3]. If the maximum signal level of $V_{R,conv}(z)$ exceeds the full range input V_{FS} of the quantizer the quantizer becomes overloaded. In most cases this will cause the modulator to become unstable. Since, the STF approximately equals one for the frequency range of interest, the full scale of the quantizer is chosen identical to that of the modulator. In such a conventional modulator the relationship between V_{FS} and Δ in the case of an L-bit quantizer equals:

$$\#comparators = \frac{V_{FS}}{\Delta} = 2^L - 1 \tag{2}$$

Hence, each reduction of Δ with a factor of two, results in a doubling of the number of comparators. In our case of a 6-bit quantizer, 63 comparators would be required.

In the designed modulator the number of comparators was greatly reduced. A key element for this was the use of the architecture of Fig. 2. In this architecture the input-output behavior of the dashed rectangular is identical to that of a normal quantizer. As such this architecture collapses to that of a conventional modulator [14]. This can be understood as follows. One can show that the output of the modulator equals:

$$\begin{aligned} D(z) = &([V_{Q1}(s)]^* - V_{Q2}(z))\, NTF(z) \\ &+ Q(z)NTF(z) + [STF(s)V_{in}(s)]^* \end{aligned} \tag{3}$$

In the architecture of Fig. 2 the signals $[V_{Q1}(s)]^*$ and $V_{Q2}(z)$ are equal. As a result the output, the performance and the signals at the internal levels of the modulator are the same as that of the conventional modulator. On the other hand, focusing on the signal at the input of the quantizer, this signal is given by:

$$V_R(z) = [V_Q(s) - V_{Q1}(s)]^* \tag{4}$$

In the proposed architecture $V_{Q1}(s)$ is derived from V_Q and operates as a good prediction of V_Q. Therefore, the signal range of $V_R(z)$ can be much smaller than the signal range at the input of the modulator. This is the basic idea of the architecture of Fig. 2. Finally, note that there is a similarity with a modulator using a two-step flash in the loop. However, in our architecture the input-output delay of the two-step flash and the power hungry analog sample&hold are avoided.

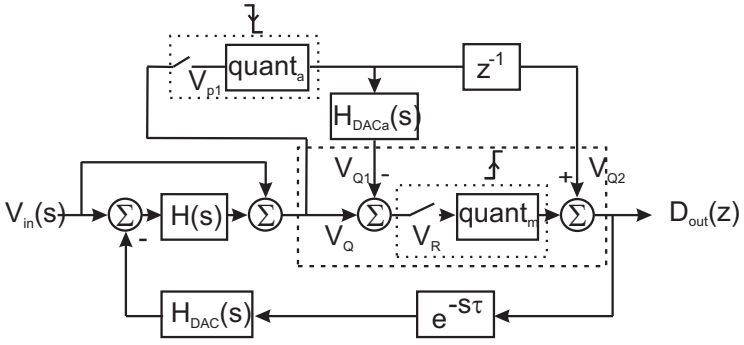

Figure 2. Modulator architecture.

To obtain the prediction signal $V_{Q1}(s)$, $V_Q(s)$ is sampled in a (low-resolution) auxiliary quantizer ($quant_a$ in Fig. 2). Next, $V_{Q1}(s)$ is found by sending this rough estimation of V_Q through an auxiliary DAC. To allow the cascade of auxiliary quantizer, auxiliary DAC and main quantizer to be defined properly, the signal $V_Q(s)$ is sampled on the falling edge of the clock and the signal V_R on the next rising edge.

Fig. 2 showed the conceptual architecture of our modulator. A drawback of this architecture is that it has two adder blocks in cascade. This increases the speed requirements on these blocks. Therefore, the actually implemented structure is slightly different and is shown in Fig. 3. Here the adder blocks are

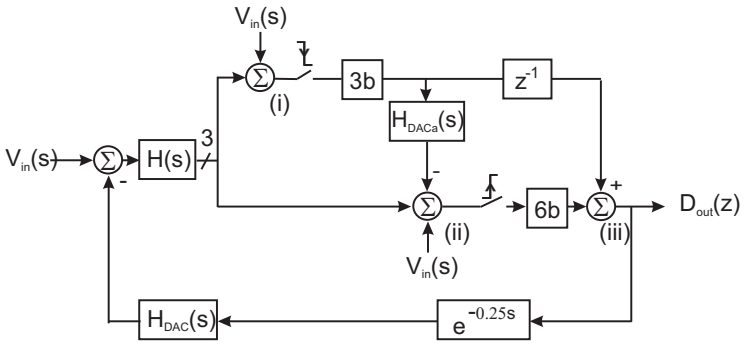

Figure 3. Implemented modulator.

rearranged to avoid this cascade. The auxiliary quantizer ($quant_a$ in Fig. 2) is a 3-bit quantizer (with quantization step Δ_a) in our design. The 3rd-order loop filter is implemented as a cascade of integrators with feedforward (shown in Fig. 4). Therefore the three integrator outputs of Fig. 4, also have to be added by the adder circuit.

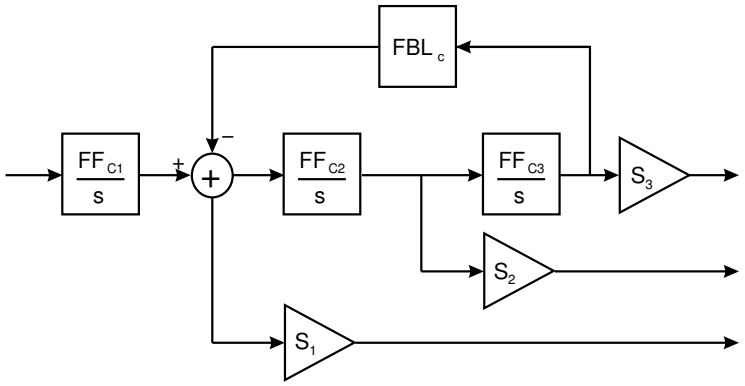

Figure 4. Modulator loopfilter.

It can be shown, by theory and by simulations, that the signal range at the input of the quantizer is covered by 10 quantization steps Δ_m [14]. To account for additional parasitic effects such as gain and/or offset errors [14], we implemented 14 comparator levels in the main quantizer. Through the use of the interpolation technique, the number of comparators was further reduced to 7 [20]. Together with the 8 comparators of the auxiliary quantizer, a total of 15 comparators were used instead of the 63 required in the conventional modulator.

3 System level design

Observing the input-output behavior of the dashed rectangular in Fig. 2 it can be seen that this behavior is identical to a conventional full-range 6-bit

quantizer. Therefore the next step in the design of our modulator is the loop filter design, to determine the value of the coefficients in the structure of fig. 4. As mentioned above, a 3rd order loop was chosen to obtain good noise shaping performance. The oversampling ratio was set to 32. This way the quantisation noise performance can be designed for a dynamic range of over 105 dB.

Usually, the design of a continuous time $\Sigma\Delta$-modulator is inspired by the discrete time variant. This means that the loop filter $H(s)$ is designed such that the equivalent discrete time loop filter $H_{eq}(z)$ equals a desired discrete time filter, say $H_{aim}(z)$. However, in our multi-bit case, both the time required for a DEM technique to linearize the DAC in the feedback path as well as the finite decision time of the quantizer add to an inevitable loop delay. As a consequence, if $H(s)$ is of third order, $H_{eq}(z)$ is of fourth order. This means that loop delay causes the described method to be unfeasible and to result in the structure lacking one degree of freedom to have full control over all the poles [16]. This problem has been solved in e.g. [13] by the introduction of an additional feedback path directly to the input of the quantizer. However, in our case this additional path is an (expensive) 6-bit DAC, making this solution less interesting. Moreover we have found that this approach requires accurate matching of the integrator's time constants relative to the clock frequency. As a result tuning or trimming of the integrator time constant is needed in practice.

Therefore, we chose to avoid the additional feedback DAC and to include the loop delay in the nominal design. To do this an explicit synchronisation is used in the feedback path to set the delay in a controlled way to 25% of the clock period. This was implemented by deriving the modulator clock frequency from a double-frequency clock and appropriately using rising and falling edges.

Next a robustly stable loop filter was designed, using the strategy described in [18]. In this approach the design is based on the Nyquist-curve of the equivalent discrete time loop filter, given by:

$$H_{eq}(z) = \mathcal{Z}\left[\mathcal{L}^{-1}\left(H(s)H_{DAC}(s)e^{-s\tau}\right)\Big|_{t=nT}\right]. \tag{5}$$

Here, τ is the loop delay which is equal to $0.25T_S$.

As is common, first, the NTF-zeros are optimized. The next step is to determine the loop filter zeros to obtain a robustly stable modulator loop. These were chosen such that the vector gain margin (VGM) of $H_{eq}(z)$ was maximized. This vector gain margin is defined as:

$$VGM = \frac{1}{1 - R_{min}}, \tag{6}$$

where R_{min} is the minimum distance of the Nyquist-curve of $H_{eq}(z)$ to the critical point -1 (see also Fig. 5). It has been shown in [18] that this VGM is

a practical way to evaluate the robust stability of the modulator. Therefore, maximizing the VGM maximizes the robust stability of the modulator. This procedure resulted in the following loopfilter:

$$H(s) = \frac{0.86(sT).^2 + 0.178(sT) + 0.087}{(sT) \cdot ((sT)^2 + (0.07605)^2)} \tag{7}$$

Here T corresponds to the sampling period. Fig. 5 gives a graphical representation of this design. On the left, the Nyquist-curve of the modulator is shown, it has a VGM of about 2. The right of the figure shows the response of the NTF. In system-level simulation, this design achieves a dynamic range of 105 dB. Note that this is about 15 dB less good than what an ideal 3rd order 6-bit design could achieve.

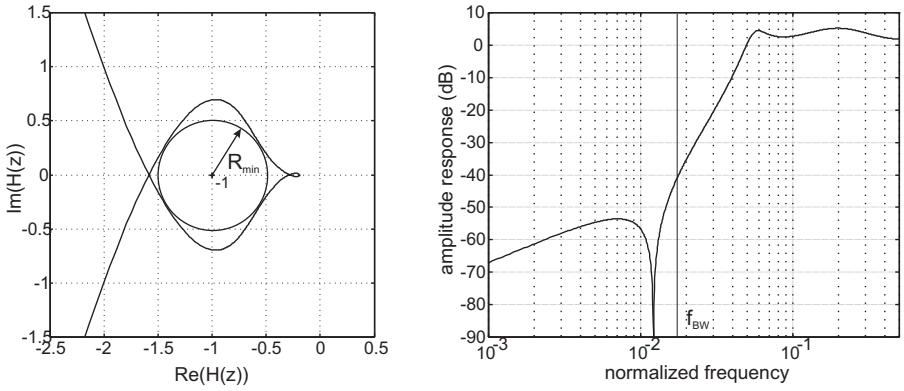

Figure 5. Detailed image of the Nyquist-curve of $H_{eq}(z)$(left). Amplitude response of the NTF (right).

4 Circuit level design

To validate these concepts a test-chip with our proposed modulator was designed in a 0.35 μm CMOS technology with four metal and two poly layers. The supply voltage was 3.3 V. A dynamic range of 95 dB was targetted for a bandwidth of 1.5 MHz. Fairly standard circuit design techniques were used for the circuits in the loop filter, which are similar to [1]. The first integrator in the loop is implemented as an RC-active integrator, using a telescopic cascode operational amplifier. The second and third integrator are implemented as g_mC-integrators with a local feedback path. Each g_m-cell consists of a differential pair, source-degenerated with a resistor, similar to [1]. The corresponding resistor and capacitor values are listed in table 1.

For the adders (i) and (ii) of Fig. 3 similar circuitry as in [13] were used. They consist of simple g_m-cells of which the output current flows through a common resistive ladder. In the special case of adder (ii) the prediction signal generated

Table 1
Component values in main circuit blocks.

	1st Integrator (RC active)	2nd Integrator (g_mC)	3rd Integrator (g_mC)
Resistor size	400Ω	6K	13K2
Capacitor size	38 pF	3.6 pF	3.6 pF

by the auxiliary quantizer is added using a current steering DAC, as shown in Fig. 6 [13]. On the ladder, signals can be tapped at several points. This way the comparator inputs can be tapped directly from the ladder [13]. In the case of Fig. 6 these points correspond to the 14 comparator levels used in the main quantizer. Each comparator consists of a pre-amplifier and a dynamic latch [21].

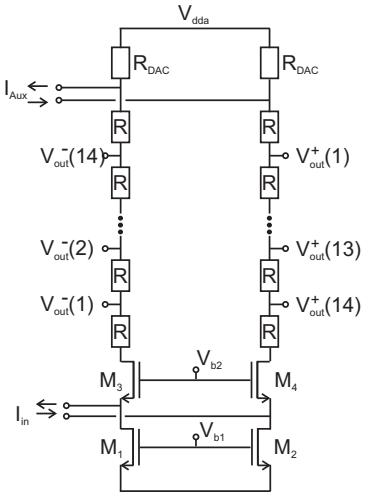

Figure 6. The resistive ladder of adder (ii) for the main quantizer.

The feedback DAC is linearized using data weighted averaging (DWA) [22]. The digital circuitry to implement the DWA has about 2.5 ns (one quarter of a clock cycle) to settle, which is set through the fixed delay in the feedback path of the loop. To achieve sufficiently fast operation this logic is implemented with transmission gate logic (TMG-logic) [23, 24]. The TMG-logic consists of shifters where a single bit input indicates whether the input code of the shifter should or should not be shifted over a fixed number of positions. In our case each shifter consists of only nMOS-transistors. This is possible, since the default output voltage of the dynamic latches is high and only transitions from high to low should ripple fast through the TMG-structure. TMG-logic was also used to realize a fast implementation of adder (iii).

Next, the output code of the TMG-array is send to an array of synchronisation latches [25] which are used to drive the DAC unit cells. The clock used for these latches is delayed over 25% of the clock period to set the loop delay in accordance to the system level design.

5 Evaluation

5.1 Simulations

During the complete design procedure the VGM was used as a key element. It was e.g. used to measure the degradation of the stability of the modulator due to parasitic effects introduced by the actual implementation of the circuit elements. Such an evaluation is illustrated in Fig. 7 and 8. Normally, designers use the Bode-diagram of $H(s)$ as shown in Fig. 7 to evaluate their design by means of e.g. the phase margin. However, in the design of a continuous time $\Sigma\Delta$-modulator the Bode-diagram of $H(s)$ does not include the transfer function of the DAC, $H_{DAC}(s)$. Even if the transfer function of the DAC is included and the Bode-diagram of $H(s)H_{DAC}(s)$ is investigated, still the sampling operation is ignored. Therefore, we used the same data used for the Bode-diagram of Fig. 7 to find the exact discrete time equivalent loop filter using:

$$H_{eq,sim}(z) = \frac{1}{T}\sum_{n=-\infty}^{n=\infty}(H(s+j2\pi f_s)H_{DAC}(s+j2\pi f_s)) \tag{8}$$

In practice this infinite sum can be broken up after about 5 terms. Using this $H_{eq,sim}(z)$ both the transfer function of the DAC as well as the sampling operation are included in the analysis.

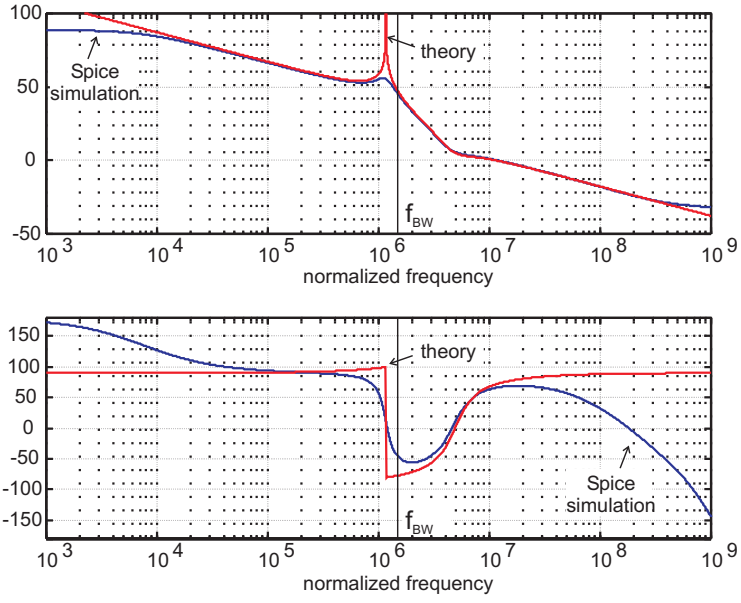

Figure 7. Bode-diagram of the theoretically designed loop filter $H(s)$ and the Spice (transistor-level) simulation of actually designed circuit.

The (robust) stability of the modulator circuit is next checked using the VGM using the Nyquist curve of $H_{eq,sim}$ as shown in Fig. 8. This figure also includes a comparison with the Nyquist curve at the system level $H_{eq}(z)$. Based upon this

figure it is concluded that due to the parasitic effects the VGM of the simulated modulator including all but the layout parasitics is reduced from 2.03 to 1.82. This is still sufficiently above the critical value of VGM=1 to leave enough margin for the modulator to be robust against other (unsimulated) parasitics and/or parameter uncertainties. Especially the latter might be important since the first integrator is of a different type compared to the last two and since no tuning mechanisms were included.

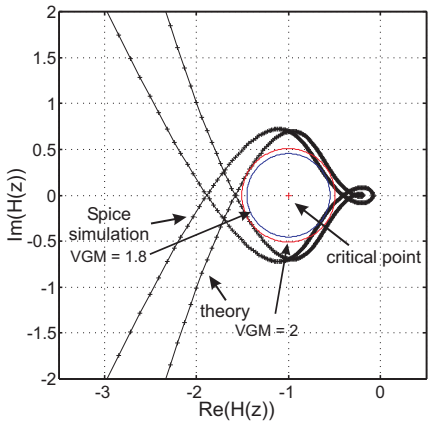

Figure 8. Comparison of the Nyquist-curve of the discrete time equivalent loop filter $H_{eq}(z)$ at the system level and in simulation.

5.2 Measurements

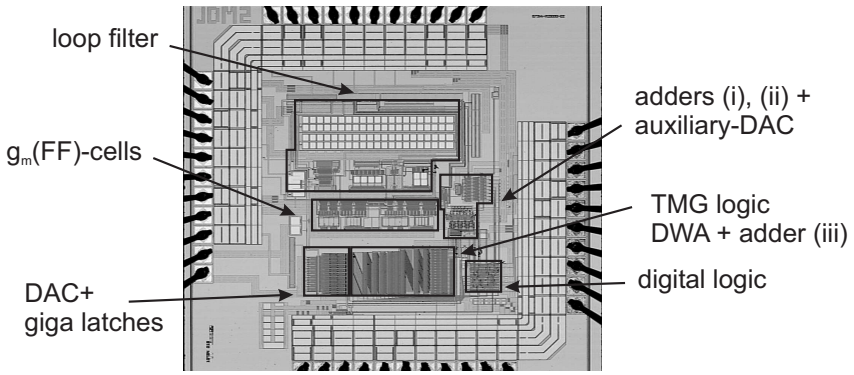

Figure 9. Microscope photo of the chip.

A microscope photo of the chip with the main circuit components indicated is shown in Fig. 9. Including the pads the chip is about 3.61 mm^2 large, the core 1.44 mm^2. The prototype was packaged in a standard 44-pins JLCC package. For the measurements it was socketed on an FR4 four-layer test board. The bandwidth of 1.5 MHz combined with an OSR of 32, leads to a sampling frequency of 96 MHz. A on-chip amplifier is used to derive all the required clock signals out of a low-level 192 MHz sinusoïdal RF input signal.

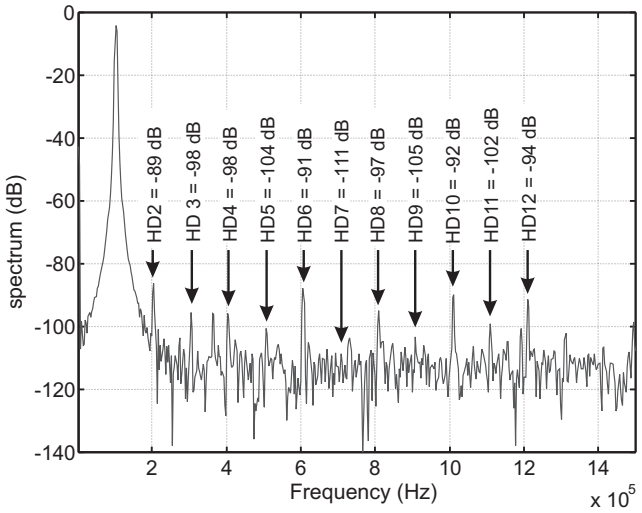

Figure 10. Spectrum of decimated signal.

A typical baseband spectrum is shown in Fig. 10. Here the modulator is driven by a 100 kHz sine wave input signal with an amplitude of 3.5 dB below the full scale. The corresponding SNR is 82 dB and the SNDR is 76 dB, which corresponds to the peak SNDR. A plot of the SNR and SNDR as a function of the input amplitude is shown in Fig. 11. From the figure, a dynamic range of 85 dB can be derived. This is clearly below our targetted value of 95 dB. The origin of this degradation is not entirely understood. It is in part attributed to digital switching noise coupling from the output pad drivers which were implemented with standard cell circuitry. This could be eliminated by using LVDS-output drivers. Additionally the SNR-plot exhibits a dip around a -15 dB input amplitude. The origin of this dip turns out to be due to the speed of adder (ii). For optimal functioning of the modulator, this adder has to settle to $\pm 3\%$ (half an lsb at the 6-bit level) in less than half the clock period (about 2.5 ns). Settling errors on this adder manifest themselves as additional noise injected at the quantiser. After evaluation, the speed of this adder turned out to be lower than expected due to layout parasitic capacitances at the taps of the resistive ladder (see fig. 6) which were underestimated in the design phase. This effect is signal dependent, because it is much more severe when the adder has to switch frequently. This happens when the amplitude of the input signal is such that the input signal remains for a long time close to a decision level of the auxiliary quantizer. In fact we were able to vary the location of the dip in the plot, by varying the offset of the input signal. A posteriori Spice simulations where the correct layout parasitics were included, confirm this mechanism. This effect could be eliminated by modifying the implementation of the adder. E.g. adding a buffer as in [26] would probably eliminate this problem.

We were able to verify that the modulator is indeed robustly stable, by observing that the modulator remains stable when the clock frequency is varied

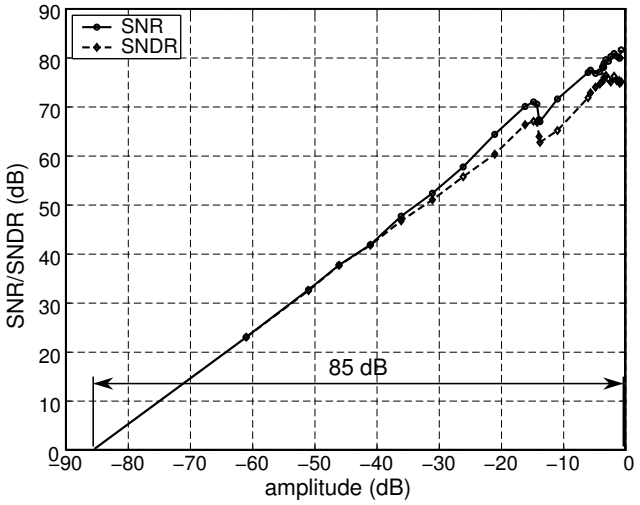

Figure 11. SNR and SNDR as a function of the input amplitude (dB).

Table 2
The main characteristics of the prototype.

Technology	0.35 μm CMOS (4M2P)
Supply voltage	3.3 V
Input range	$\pm$1 Volt diferentially
Sampling frequency	96 MHz
Bandwidth after reconstruction	1.5 MHz
Measured power consumption	54 mW Analog
	17 mW Clock amplifiers and buffers
Peak SNDR	76 dB
Peak SNR	82 dB
Dynamic range	85 dB

over more than 20 % of its nominal value. This confirms the validity of the Nyquist criterion based design of the loop filter.

The main characteristics of the test chip are summarized in table 2.

6 Conclusion

In this paper we presented a continuous time $\Sigma\Delta$-modulator. Through the combination of a modified architecture and comparator interpolation, it only requires a total of 15 comparators to implement a 6-bit quantiser. However, it was found that this modification requires a high-speed analog adder.

Additionally, it was demonstrated that the Nyquist stability criterion and the vector gain margin can be used to design robustly stable continuous time modulators. The prototype modulator has a dynamic range of 85 dB and a peak SNR/SNDR of 82dB/76dB respectively over a 1.5 MHz bandwidth.

Acknowledgment

J. De Maeyer was supported by a fellowship of the Fund for Scientific Research - Flanders (F.W.O.-V., Belgium). He is currently with AMISemiconductor Belgium, Oudenaarde, Belgium.

References

[1] L. Breems, E. van der Zwan and J. Huijsing, "A 1.8-mW CMOS $\Sigma\Delta$ Modulator with integrated Mixer for A/D Conversion of IF signals," IEEE J. Solid-State Circuits, vol. 35, No. 4, pp. 468-475, Apr. 2000.

[2] E. van der Zwan, K. Philips and C. Bastiaansen, "A 10.7-MHz IF-to-Baseband $\Sigma\Delta$ A/D Conversion System for AM/FM Radio Receivers," IEEE J. Solid-State Circuits, vol. 35, No. 12, pp. 1810-1819, Dec. 2000.

[3] J. De Maeyer, J. Raman, P. Rombouts, and L. Weyten, "Controlled Behavior of the STF in CT $\Sigma\Delta$ Modulators," IEE Electronics Letters, vol. 41, no. 16, pp. 19–20, Aug. 2005.

[4] R. van Veldhoven, "A triple-mode continuous-time Sigma Delta modulator with switched-capacitor feedback DAC for a GSM-EDGE/CDMA2000/UMTS receiver," IEEE J. Solid-State Circuits, vol. 38, No. 12, pp. 2069-2076, Dec. 2003.

[5] J. Cherry and W. Snelgrove, "Clock jitter and quantizer metastability in continuous-time deltasigma modulators," IEEE Trans. Circuits Syst.-II, Analog Digit. Signal Process., vol. 46, no. 6, pp. 661676, Jun. 1999.

[6] K. Reddy and S. Pavan, "Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter," IEEE Trans. Circuits Syst.-I, vol. 54, No. 10, pp. 2184-2194, Oct. 2007

[7] L. Hernandez, A. Wiesbauer, S. Paton, and A. D. Giandomencio, "Modelling and optimization of low-pass continuous-time Sigma-Delta modulators for clock jitter noise reduction," in Proc. IEEE Int. Symp. Circuits Syst .(ISCAS), May 2004, vol. 1, pp. I-1072-1075.

[8] M. Ortmanns, Y. Manoli, and F. Gerfers, "A continuous-time sigma- delta modulator with reduced jitter sensitivity," in Proc. 28th ESSCIRC, Sep. 2002, pp. 287-290.

[9] M. Ortmanns, F. Gerfers, and Y. Manoli, "A Continuous-Time ΣΔ Modulator with Reduced Sensitivy to Clock Jitter through SCR Feedback," IEEE Trans. Circuits Syst.-I, vol. 52, no. 5, pp. 875–884, May 2005.

[10] A. Latiri, H. Aboushady, and N. Beilleau, "Design of Continuous-Time Sigma-Delta Modulators with Sine-Shaped Feedback DACs," in Proc. IEEE Int. Symp. on Circ. and Syst. (ISCAS), Kobe, Japan, 23-26 May 2005, vol. 4, pp. 3672–3675.

[11] G. Mitteregger, et al. "A 20-mW 640-MHz CMOS continuous-time Sigma Delta ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," IEEE J. Solid-State Circuits, vol. 41, No. 12, pp. 2641-2649, Dec. 2006

[12] S. Yan and E. Sánchez-Sinencio, "A Continuous-Time ΣΔ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," IEEE J. Solid-State Circuits, vol. 39, no. 1, pp. 75–86, Jan. 2004.

[13] S. Patón, A. Di Giandomenico, L. Hernàndez, A. Wiesbauer, T. Pötscher, and M. Clara, "A 70-mW 300-MHz CMOS Continuous-Time ΣΔ ADC with 15-MHz Bandwidth and 11 Bits of Resolution," IEEE J. Solid-State Circuits, vol. 39, no. 7, pp. 1056–1063, Jul. 2004.

[14] J. De Maeyer, P. Rombouts and L. Weyten, "Efficient Multibit Quantization in Continuous-Time ΣΔ Modulators," IEEE Trans. Circuits Syst.-I, vol. 54, No. 4, pp. 757-767, Apr. 2007

[15] S. Kwon and F. Maloberti, "Op-Amp Swing Reduction in Sigma-Delta Modulators," in Proc. IEEE Int. Symp on Circuits Syst. 2004, May 2004, pp. 525-528.

[16] J. Cherry and W. Snelgrove, "Excess loop delay in continuous-time delta-sigma modulators," IEEE Trans. Circuits Syst.-II, Analog Digit. Signal Process., Vol. 46, No. 4, pp. 376-389, Apr. 1999.

[17] P. Benabes, M. Keramat and R. Kielbasa, "Synthesis and analysis of sigma-delta modulators employing continuous-time filters," Analog Int. Circuits and Signal Process., vol. 23, no. 2, pp. 141-152, 2000.

[18] J. De Maeyer, P. Rombouts and L. Weyten, "Nyquist criterion based design of continuous time ΣΔ-modulators,". Proc. of the IEEE Int. Symp. on Circuits and Systems (ISCAS). 2006. pp. 2501-2504

[19] J. Silva, U. Moon, J. Steensgaard and G. Temes, "Wideband low-distortion delta-sigma ADC topology," Electron. Lett., vol. 37, No. 12, 737-738, 7th Jun. 2001

[20] K. Kim, N. Kusayanagi and A. Abidi, "A 10-b, 100-MS/s CMOS A/D Converter," IEEE J. Solid-State Circuits, vol. 32, No. 3, pp. 302-311, Mar. 1997

[21] P. Rombouts, J. De Maeyer and L. Weyten, " A 250-kHz, 94-dB double-sampling ΣΔ modulation A/D converter with a modified noise transfer

function," IEEE J. Solid-State Circuits, vol. 38, No. 10, pp. 1657-1662, Oct. 2003.

[22] R. Baird and T. Fiez, "Linearity Enhancement of Multibit $\Delta\Sigma$ A/D and D/A Converters Using Data Weighted Averaging," IEEE Trans. Circuits Syst.-II, vol. 42, No. 12, pp. 753-762, Dec. 1995.

[23] A. Hamoui, K. Martin, "High-order multibit modulators and pseudo data-weighted-averaging in low-oversampling Delta Sigma ADCs for broad-band applications," IEEE Trans. Circuits Syst.-I, vol. 51, No. 1, pp. 72-85, Jan. 2004

[24] M. Miller and G. Petrie, "A Multibit Sigma-Delta ADC for Multimode Receivers," IEEE J. Solid-State Circuits, vol. 38, no. 3, pp. 475–782, Mar. 2003.

[25] A. Van den Bosch, M.A.F. Borremans, M.S.J. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 315–324, Mar. 2001.

[26] L. Breems, R. Rutten, G. Wetzker, "A cascaded continuous-time Sigma Delta modulator with 67-dB dynamic range in 10-MHz bandwidth," IEEE J. Solid-State Circuits, vol. 39, No. 12, pp. 2152-2160, Dec. 2004